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Long Time-Constant Trap Effects in Nitride Heterostructure Field Effect Transistors

Xiaozhong Dang[1], Peter M. Asbeck[1], Edward T. Yu[1], Karim S. Boutros[2,a], Joan M. Redwing[2,b]
[1]Department of Electrical and Computer Engineering, University of California at San Diego, 9500 Gilman Drive, La Jolla, CA 92093-0407
[2]Epitronics/ATMI, 21002 north 19th Avenue, Suite 5, Phoenix, Arizona 85027-2726
[a]Currently: Spectrolabs, 12500 Gladstone Ave., Sylmar, CA 91343
[b]Currently: Department of Materials Science and Engineering, Pennsylvania State University, University Park, PA 16802

ABSTRACT

Current collapse effects in an $Al_{0.25}Ga_{0.75}N$/GaN HFET have been investigated under pulsed bias conditions, and a detailed investigation of current responses to changes in drain or gate bias voltage (drain-lag and gate-lag, respectively) has been performed. Three components of transient current response to changes in drain and gate bias voltages are distinguished. Surface treatment using KOH etching and the influence of pulsed bias conditions on threshold voltage are investigated to explore the origins of traps associated with each current transient component.

INTRODUCTION

AlGaN/GaN heterostructure field-effect transistors (HFET's) have attracted intense research interest due to their outstanding potential for operation at high power, high temperature, and high frequency [1-4]. Despite the attainment of extremely high power densities and total power at microwave frequencies, the microwave power densities reported are often lower than those that would be expected based on measured direct-current (dc) current-voltage (*I-V*) characteristics [3,4]. Reductions in current flow, i.e. current collapse, and power have also been observed under pulsed bias conditions in GaN field-effect transistors (FET's) and high-electron-mobility transistors (HEMT's), and were attributed to traps in these devices [5,6]. A detailed assessment of these effects and characterization of the relevant trap states is crucial for optimization of nitride transistor performance.

EXPERIMENT

The HFET structure employed in this study was grown on a c-plane (0001) sapphire substrate by low-pressure metalorganic vapor phase epitaxy, and consisted of a 300 Å nominally undoped $Al_{0.25}Ga_{0.75}N$ barrier layer grown on a 3 μm undoped highly resistive GaN layer. A two-dimensional electron gas (2DEG) is formed at the $Al_{0.25}Ga_{0.75}N$/GaN interface due to the presence of polarization charges [7] and background doping in the $Al_{0.25}Ga_{0.75}N$ layer. Transistors were fabricated using Ti/Al to form the source and drain Ohmic contacts and Ni/Au to form the gate Schottky contact. In these devices, the gate length is 1 μm, the gate width is 25 or 50 μm, the source-drain spacing is 3 μm, and the gate-drain spacing is approximately 1 μm. A more detailed description of the fabrication and dc characterization of these devices can be found elsewhere [8].

I-V characteristics of these devices were measured under both dc and pulsed bias conditions. Significant current collapse effects were observed under both pulsed drain and pulsed gate bias conditions. The mechanisms responsible for the observed current collapse effects were studied

by measuring the drain-current transient response to changes in drain bias or gate bias voltage — so-called "drain-lag" or "gate-lag" effects, respectively. The influences of surface treatment with hot KOH solvent on the transient current response and of pulsed bias voltages on the threshold voltage were also investigated. These studies provided information concerning the locations of traps responsible for various transient current effects.

DISCUSSION

Current collapse under pulsed bias conditions

Figures 1 (a) and (b) show the *I-V* characteristics of an undoped $Al_{0.25}Ga_{0.75}N$ /GaN HFET under pulsed drain bias voltage and pulsed gate bias voltage, respectively, with *I-V* characteristics measured under dc conditions shown for comparison. The threshold voltage is around –3 V. In both cases, the pulse duration is 1 ms with a period of 10 ms. The base voltage for pulsed drain bias is 20 V, and the base voltage for pulsed gate bias is –10 V. Significant current collapse under both pulsed drain and pulsed gate bias voltage conditions can be seen, consistent with the reported current collapse and power compression effects under ac conditions [3,6,9]. In order to distinguish between heating and trap effects in our pulsed drain bias voltage measurements, the pulsed bias measurements were also performed with additional illumination incident on the device; the results are shown by the dashed lines in Figure 1. Under illumination, the *I-V* characteristics obtained under pulsed bias condition recover to nearly the levels observed in dc measurements, suggesting that the current collapse effects arise largely due to the presence of traps.

Drain lag and gate lag measurements

A typical drain lag measurement is depicted in Figure 2. The device is initially biased with a drain-source voltage V_{DS} of 4 V and a gate-source voltage V_{GS} of 0 V until the current becomes stable (region a). The drain-source voltage is then changed to 20 V for around 100 s (region b), and finally restored to its original value of 4 V (region c). The same charge trapping processes are responsible for the transient current behavior in both region (b) and region (c), and we will

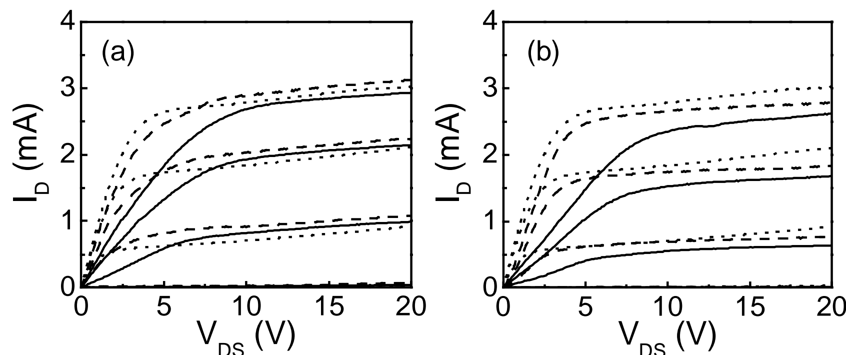

Figure 1. *The I-V characteristic of an undoped $Al_{0.25}Ga_{0.75}N$/GaN HFET under (a) pulsed drain bias and (b) pulsed gate bias conditions. The solid and dashed lines indicate current measured under pulsed bias conditions in room light and with additional illumination, respectively. The dc characteristics are plotted using dotted lines for comparison. Values for gate bias V_{GS} are (from top to bottom) 0 V, -1 V, -2 V, -3 V.*

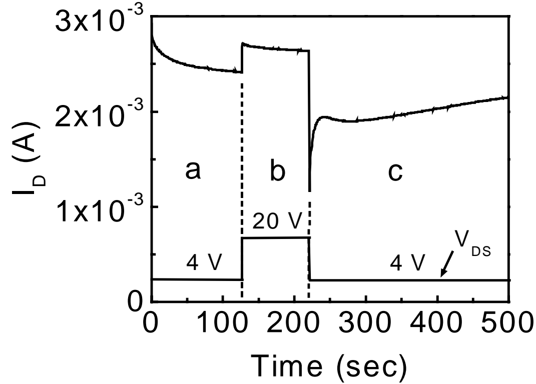

Figure 2. *Typical drain lag measurement of an undoped $Al_{0.25}Ga_{0.75}N/GaN$ HFET. The applied bias V_{DS} and the resulting current I_D are plotted as a function of time. $V_{GS} = 0$ V during the measurement. Multiple transient components are observed in I_D when V_{DS} is changed from 20 V to 4 V.*

therefore focus primarily on the behavior observed in (c). It is evident from Figure 2 that the transient current response to a change in V_{DS} from 20 V to 4 V contains three principal components: a substantial increase in current with a time constant of order ~ 1 s, a transient decrease in current with a time constant of order ~ 10 s, and finally a gradual increase in current to its steady-state value with a time constant of hundreds of seconds or longer. In the following, these components are referred to as “fast”, “intermediate”, and “slow”, respectively. The observation of different transient current components over several time scales is indicative of the presence of a variety of trap states located in different regions within the HFET device structure.

The transient response in drain current to changes in V_{DS} and V_{GS} varies strongly with the size of the change in applied voltage. Figure 3 shows the transient drain-current response to a change in V_{DS} to 4 V from initial voltages ranging from 9 V to 24 V, for a constant gate-source voltage $V_{GS} = 0$ V, i.e., a drain-lag measurement. For an initial value of V_{DS} of 9 V, the “fast” transient current component is largely absent, while the “intermediate” and “slow” components are present to moderate degrees. The “fast” and “slow” transient current components increase steadily in amplitude with increasing initial V_{DS}, while the “intermediate” component appears to vary little with V_{DS}.

The transient current responses observed here are similar to those previously measured in III-V compound semiconductor FET’s [10-13], suggesting that charge trapping effects in our nitride devices may be analogous to those observed previously in other material systems. The “fast” and “slow” transient current components observed in our studies increase in amplitude with increasing V_{DS}. The signs of these transient current components are consistent with trapping of electrons in deep-level states near the HFET channel, i.e., at the AlGaN surface, in the AlGaN barrier, at the AlGaN/GaN interface, or in the GaN buffer layer, in the region between the gate and drain contacts. Analogous effects and proposed charging mechanisms have been reported for InP-based HFET’s [10] and GaAs FET’s [11]. Concurrently, the application of large drain-source bias voltages can deplete normally-filled deep-level traps in the region between the gate and drain contacts, especially near the drain edge of the gate. The resulting positive charge will cause a transient current response similar to the “intermediate” transient observed upon reduction of V_{DS}. Similar effects and proposed charge-trapping mechanisms have been reported for AlGaAs/GaAs HFET’s [12,13]. The observation in our studies that the “intermediate” transient response does not increase in amplitude with increasing V_{DS} suggests that the trap states are located primarily in the AlGaN barrier, as simulations have indicated that the vertical potential distribution within the barrier at the drain edge of the gate varies little over the range of voltages employed in our measurements.

Figure 4 shows the transient drain-current response to a change in V_{GS} to 0 V at time $t = 0$ from negative values ranging from –1 V to –10 V, for a constant drain-source voltage $V_{DS} = 3$ V,

i.e., a gate-lag measurement. For initial values of V_{GS} above the threshold voltage of –3.2 V, there is a small current overshoot and a transient decrease with a time constant consistent with the "intermediate" transient seen in Figure 3. The sign of this transient response observed in Figure 4 is consistent with the sign and physical mechanism proposed for the "intermediate" transient observed in the drain-lag measurement, as described above. For initial values of V_{GS} below the threshold voltage, transient currents are observed that are consistent in sign and time scale with the "fast" and "slow" transients observed in response to changes in V_{DS}. Furthermore, the variations in amplitude of the transient components observed in the gate-lag measurements shown in Figure 4 suggest that they arise from the same physical charge trapping mechanisms postulated to give rise to the transient response observed in the drain-lag measurements shown in Figure 3.

Influence of surface treatment on current lag effects

In order to investigate the relationship between the observed transient current effects and surface properties of the $Al_{0.25}Ga_{0.75}N$/GaN HFET structure, some devices were etched in hot (~ 90°C) KOH:H_2O (1 mol/L) solution for ~ 10 s. KOH solutions have been reported to etch the GaN surface oxidation layer and improve GaN/metal contact properties [14]. The drain-lag and gate-lag effects were measured both immediately after and two days after etching in the KOH solution. Figures 5 (a) and (b) show comparisons of current transients immediately and two days after etching for drain-lag and gate-lag, respectively. For both the drain and gate lag effects, there are significant increases in the magnitude of the "fast" transient components two days after etching, but very little change in the "intermediate" and "slow" transient components. These results suggest that the "fast" component of the transient current is probably related to surface trap states, the presence and nature of which may have been altered by the initial KOH etch and subsequent exposure of the etched device surface to air for an extended period. The observed behavior of the "intermediate" transient component is consistent with our explanation that it

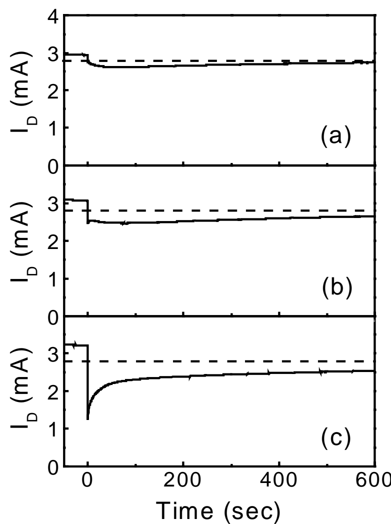

Figure 3. *Transient response in drain current to change in V_{DS} to 4 V from (a) 9 V, (b) 14 V and (c) 24 V. V_{GS} is fixed at 0 V during the measurement. The dashed lines are the stabilized current levels for $t \rightarrow \infty$.*

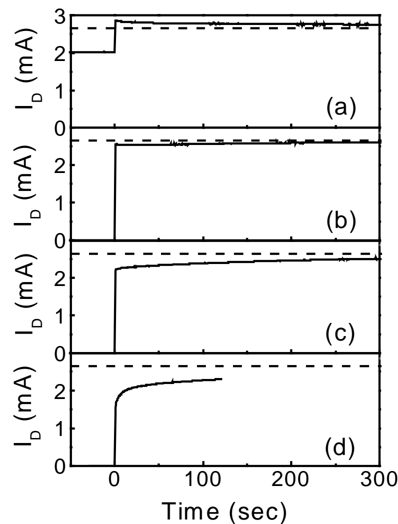

Figure 4. *Transient response in drain current to change in V_{GS} to 0 V from (a) -1 V, (b) -3.5 V, (c) -6 V and (d) -10 V (d). V_{DS} is fixed at 3 V during the measurement. The dashed lines are the stabilized current levels for $t \rightarrow \infty$.*

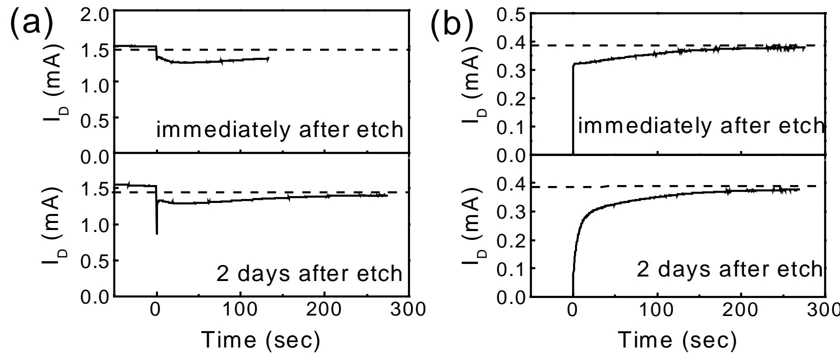

Figure 5. (a) *drain-lag and (b) gate-lag response, immediately and 2 days after etching in KOH. In (a), V_{DS} is changed from 20 to 4 V with V_{GS} = 0 V; in (b), V_{GS} is changed from –10 to 0 V with V_{DS} = 3 V. The dashed lines are stabilized current levels at $t \rightarrow \infty$.*

arises from traps in the AlGaN barrier layer, which should not be strongly affected by the KOH etch. Similarly, the observed behavior of the "slow" transient component suggests that it also arises from traps which are not strongly affected by KOH etch, and thus are likely to be located under the surface.

Threshold voltage under pulsed conditions

Further information about the location of the traps responsible for drain-lag and gate-lag effects can be obtained from influence of pulsed bias conditions on the threshold voltage. The saturated drain-current as a function of V_{GS} was measured under dc, pulsed drain bias and pulsed gate bias conditions, respectively. The results are depicted in Figure 6. In these measurements, the drain-source bias voltage is 8 V, with a pulse duration of 1 ms and a period of 10 ms. The base voltage for pulsed drain bias is 20 V, and the base voltage for pulsed gate bias is –10 V. It can be seen in Figure 6 that pulsed drain bias does not shift the threshold voltage relative to its value under dc bias conditions, while pulsed gate bias reduces the threshold voltage by ~ 0.15 V. This reduction in threshold voltage indicates that electrons are trapped in the vicinity of the channel for large negative gate bias voltages, which is consistent with the trapping behavior believed to be responsible for the "fast" and "slow" transient components in the gate lag effects. In a HFET, only charges located under the gate can cause a shift in threshold voltage. Thus, it appears that the traps contributing to the gate lag effects are at least partly located under the gate in the vicinity of the channel, while the traps contributing to the drain lag effects, which do not cause a significant change in the threshold voltage, are primarily located laterally in the region

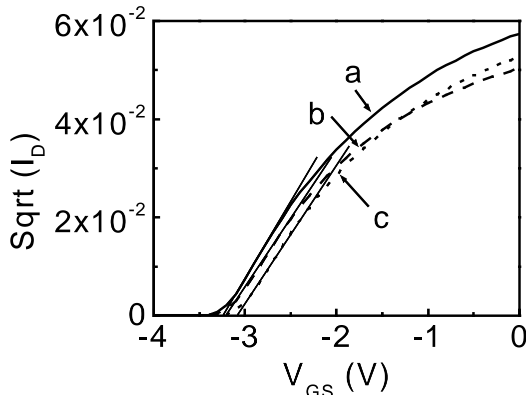

Figure 6. *Square-root of drain current as a function of gate bias voltage under (a) dc, (b) pulsed drain bias and (c) pulsed gate bias voltage conditions. In all cases I_D is measured with V_{DS} = 8 V.*

between the gate and drain/source contacts.

CONCLUSIONS

Current collapse effects in an $Al_{0.25}Ga_{0.75}N$/GaN HFET have been characterized under pulsed measurement conditions, with detailed investigations of both drain-lag and gate-lag effects having been performed. Transient current responses in drain-lag and gate-lag effects contain three principal components — "fast", "intermediate", and "slow" transients with time constants of order ~ 1 s, ~ 10 s, and hundreds of seconds, respectively. Detailed measurement and analysis of drain-lag and gate-lag effects as functions of bias pulse amplitude indicated that the "intermediate" transient component originates from deep levels in the AlGaN barrier layer. The "fast" and "slow" transient components are of opposite sign relative to the "intermediate" transient, and the "fast" component changes significantly upon etching in KOH, indicating that it is related to the presence of surface traps. The "slow" transient component varies little upon etching in KOH, and appears to arise from traps under the surface in the vicinity of channel.

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